REMARKS

Claim 2 has been amended to include a period.

Claims 1-19 have been rejected under 35 U.S.C. 102(e) as being anticipated by Kraus et al. (U.S. Patent 6,587,979).

Claim 1 recites "a plurality of random access memory (RAM) blocks … a plurality of test modules, each being coupled to a corresponding one of the RAM blocks, … and a dedicated test bus coupled to each of the test modules."

The Examiner does not indicate which elements of Kraus et al. correspond with the recited elements of Claim 1. The rejection simply cites the entire detailed description (i.e., 'col. 5 line 7 et seq.') and nine of the figures (i.e., Figs. 5-12, 16), without any indication as to how this material corresponds with the claim elements. The rejection is therefore prima facie inadequate.

The Examiner replicates Fig. 12 of Kraus et al. in the Office Action, thereby indicating that this figure has particular relevance to the rejection of Claims 1-19. However, Fig. 12 of Kraus et al. fails to teach or suggest "a plurality of test modules, each being coupled to a corresponding one of the RAM blocks" as recited by Claim 1. In addition, Fig. 12 of Kraus et al., which illustrates a different bus coupled to each of RAMs 12, teaches away from "a dedicated test bus coupled to each of the test modules" as recited by Claim 1.

The Examiner also replicates the first paragraph of the summary of Kraus et al. in the Office Action. (Kraus et al., Col. 2, lines 42-50.) This paragraph identifies "internal test circuits" which can be connected to test "RAMs". Assuming, for the sake of argument only, that the "internal test circuits" and "RAMs" recited by Kraus et al.

correspond with "test modules" and "RAM blocks" as recited in Claim 1, this section of Kraus et al. still fails to teach "a dedicated test bus coupled to each of the test modules" as recited by Claim 1.

For these reasons, Claim 1 is allowable over Kraus et al.. Claims 2-10, which depend from Claim 1, are allowable over Kraus et al. for at least the same reasons as Claim 1.

Claim 11, which recites "accessing the RAM blocks through a dedicated test bus during a test mode to test the functionality of the RAM blocks prior to normal operation of the chip", is allowable over Kraus et al. for at least the same reasons as Claim 1. Claims 12-19, which depend from Claim 11, are allowable over Kraus et al. for at least the same reasons as Claim 1.

In addition, Claim 2 recites "a switching structure" "configured to alternately couple the plurality of pads to the dedicated test bus and the system circuitry". Similarly, Claim 14 recites "coupling the pads to the system circuitry during normal operation of the chip; and coupling the pads to the test bus during the test mode." Applicant does not believe that Kraus et al. teaches "a switching structure" as recited by Claim 2 or "coupling the pads" as recited by Claim 14. If the Examiner believes that Kraus et al. teaches these elements of Claims 2 and 14, he must specifically indicate where these elements are taught by Kraus et al..

In addition, Claim 4 recites "the plurality of RAM blocks comprise dual-port and two-port RAM blocks". Similarly, Claim 17 refers to 'RAM blocks having more than one write port". Applicant does not see where Kraus et al. teaches dual-port or two-port RAM blocks. Rather, Kraus et al. seems to teach a single port RAM block. (See, e.g.,

Kraus et al., Fig. 5.) The Examiner should indicate where Kraus et al. teaches dual-port or two-port RAM blocks as recited by Claims 4 and 17.

In addition, Claim 5 recites "the dedicated test bus comprises: a first set of lines for transmitting address and data signals to the test modules; a second set of lines for transmitting command signals to the test modules; and a third set of one or more lines for transmitting a signal for latching the command signals". Applicant does not see where Kraus et al. teaches a dedicated test bus having the features recited in Claim 5. If the Examiner believes that Kraus et al. teaches a dedicated test bus having the features recited by Claim 5, he must specifically indicate where these features are taught by Kraus et al.. Similar arguments are applicable to Claims 6 and 7.

In addition, Claim 8 recites "wherein each of the test modules comprises a register for storing a unique address." Similarly, Claim 13 recites "storing a unique address in each of the test modules". Applicant does not believe that Kraus et al. teach these limitations of Claims 8 and 13. In fact, Kraus et al. relies on serially shifting data between the core wrappers 24 and the tester 21. (See, e.g., Kraus et al., Col. 10, lines 55-61; Col. 12, lines 8-11.) If the Examiner believes that Kraus et al. teaches "a register for storing a unique address" as recited by claim 5 or "storing a unique address" as recited by Claim 13, he must specifically indicate where these features are taught by Kraus et al..

In addition, Claim 16 recites "writing test data values to the RAM blocks by broadcasting the test data values to all of the RAM blocks on the test bus". In contrast, Kraus

et al. teaches that test data is provided locally by each core wrapper 24. (Kraus et al., Col. 9, lines 14-17.)

Claim 16 also recites "reading test data values from the RAM blocks by individually accessing the RAM blocks on the test bus". In contrast, Kraus et al. teaches that the test data is read (and compared) locally within each core wrapper 24. (Id.) Any test data routed from the core wrappers 24 to the tester 21 are transferred by serial shifting the test data (see, e.g., Kraus et al., Col. 10, lines 55-61; Col. 12, lines 8-11), and not by individually accessing the core wrappers 24.

For these additional reasons, Claim 16 is allowable over Kraus et al..

In addition, Claim 18 recites 'operating the test bus in response to a first clock signal during the test mode; and operating the RAM blocks in response to a second clock signal during the test mode, wherein the first clock signal and the second clock signal are independent signals.' Claim 19 recites "adjusting edges of the first clock signal relative to edges of the second clock signal". Applicant does not believe that Kraus et al. teaches these limitations of Claims 18 and 19. If the Examiner believes that Kraus et al. teaches the recited features of Claims 18 and 19, he must specifically indicate where these features are taught by Kraus et al..

Claims 1-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Jamal (U.S. Patent No. 5,568,437) in view of Kraus et al..

Claim 1 recites "a plurality of random access memory (RAM) blocks", "a plurality of test modules, each being

coupled to a corresponding one of the RAM blocks" and "a dedicated test bus coupled to each of the test modules".

As described in Applicant's Response to the First Office Action, Jamal fails to teach "a plurality of random access memory (RAM) blocks" and a corresponding "plurality of test modules" as recited by Claim 1. Also, as described in Applicant's Response to the First Office Action, Applicant indicated the reasons why it would not be obvious to simply multiply the BIST circuit 100 and RAM block 84 taught by Jamal. In addition, Applicant's Response to the First Office Action indicates the reasons why Jamal does not teach or suggest "a dedicated test bus coupled to each of the test modules" as recited by Claim 1. Applicant renews these arguments in the present Response.

The Examiner indicates that Kraus et al. remedies the deficiencies of Jamal. However, as described above, Kraus et al. fail to teach or suggest "a dedicated test bus coupled to each of the test modules" as recited by Claim 1. Thus, Kraus et al. does not remedy the deficiencies of Jamal.

For the above-described reasons, Claim 1 is allowable over Jamal in view of Kraus et al. Claims 2-9, which depend from Claim 1, are allowable over Jamal in view of Kraus et al. for at least the same reasons as Claim 1.

Claims 10-19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Jamal and Kraus et al. and further in view of Grider et al. (U.S. Patent No. 5,515,540).

Claim 10, which depends from Claim 1, is allowable over Jamal and Kraus et al. for at least the same reasons as Claim 1. Grider et al. fail to remedy the deficiencies of

Jamal and Kraus et al. Thus, Claim 10 is allowable over Jamal and Kraus et al. in view of Grider et al.

In addition, Claim 10 recites "wherein each of the RAM blocks has a capacity of 32 Kb or less".

The Examiner concludes that it would have been obvious to one by using a RAM with a limited capacity, because one of ordinary skill in the art would easier use the smaller RAM's capacity in order to achieve higher reliability.

However, as described in the specification as originally filed, RAM blocks having a capacity of 32 kb or less do not typically include associated BIST circuitry. (Specification, paragraph [0005].) As a result, RAM blocks of this size are typically not tested, or are tested with significant difficulty. (Specification, paragraph [0003].) Thus, contrary to the Examiner's assertion, it would not be obvious to use a plurality of RAM blocks "with a limited capacity" in combination with corresponding test modules. For this additional reason, Claim 10 is allowable over Jamal and Kraus et al. in view of Grider et al.

Claim 11 recites "accessing the RAM blocks through a dedicated test bus during a test mode to test the functionality of the RAM blocks prior to normal operation of the chip". As described in Applicant's Response to the previous Office Action, Jamal and Grider et al. fail to teach or suggest a dedicated test bus as recited by Claim 11. As described above, Kraus et al. also fail to teach a dedicated test bus as recited by Claim 11. For these reasons, Claim 11 is allowable over Jamal and Kraus et al. in view of Grider et al.

Claims 12-19, which depend from Claim 11, are allowable over Jamal and Kraus et al. in view of Grider et al. for at least the same reasons as Claim 11.

Applicant has added new Claims 20-22. Support for these claims is found in the specification as originally filed. No new matter is added.

CONCLUSION

Claims 1-22 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested. If the Examiner has any questions or comments, he is invited to call the undersigned.

Respectfully submitted,

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June 8, 2005 Carrie Reddick
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